

REMARKS

Amendments to the Specification correct errors without introducing new matter prohibited under 35 USC §132. On page 6, the PAL and SAL were incorrectly referenced as “101” and 201,” whereas the correct designations in Fig. 2 are “201” and “202,” respectively. The reference to “OS 103” is deleted, because second-category errors are said to be corrected with “firmware,” whereas the operating system (OS 203) corrects errors in the third category, as noted on page 7 lines 12-13. The changes on page 11 change two words that are obviously incorrect: “effect” to “affect,” and “error” to “processor.”

Claims 46-56 include systems having at least one processor in which firmware that implements abstraction layers for model specific hardware and particular platform chipset hardware also implement cooperative error handling routines. This hardware is described, inter alia, on page 5:5-15.¹ The “error correct” hardware to correct category one errors is described at page 6:19-25. Page 6:18-7:8 describe the two error categories recited in this claim. The role of the PAL firmware in claim 47 is described on page 5:6-8, while page 5:9-12 describe the SAL firmware in claim 49. Fig. 2 elements 201 and 204 depict the relationship recited in claim 48. The “system memory” of claim 53 is shown as 540 in Fig. 5, and its pertinent characteristics are described at page 16:7-8.

Claims 57-71 concern the processing of machine check abort conditions, introduced on page 5:20-6:3. Page 6:18-7:25 delineates four categories of errors. The “firmware” contains code that implements one or more abstraction layers, as noted above.

Claims 72-77 are drawn more specifically to processing systems having more than a single processor, described on page 2:12-13, which normally execute multiple different processes concurrently, as noted on page 2:22-23. Claims 78-88 concern multi-processor methods and articles related to machine check abort handling, page 5:20-6:3. The “rendezvous state” of claims 81-82 is described on page 9:28-10:5 and on page 13:21-26. The latter passage also defines the term monarch processing element or monarch processor in the claims.

¹ --- The colon notation signifies page and line numbers in the Specification. Hence, “page 5:10-12” signifies page lines 10 through 12.

PRELIMINARY AMENDMENT

Serial Number: 10/628,769

Filing Date: July 28, 2003

Title: SYSTEM ABSTRACTION LAYER, PROCESSOR ABSTRACTION LAYER, AND OPERATING SYSTEM ERROR HANDLING

Assignee: Intel Corporation

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Dkt: 884.205US2-(INTEL)

Conclusion

The amendments to the Specification and claims are thus fully supported by the Specification as originally filed, and no new matter has been added. The amendments to the claims are not intended to limit the scope of equivalents to which any claim element may be entitled. Applicant respectfully requests consideration of the above-identified Application in view of the amendments above.

The Examiner is invited to contact Applicant's representative at (612) 373-6971 if prosecution may be assisted thereby.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully Submitted,

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CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18th day of January 2005.

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